ELECTRON BEAM INDUCED CURRENT ISOLATION TECHNIQUES

By Michael Strizich

Failure Analysis of semiconductor devices gets harder as their basic dimensions shrink and their gate counts grow.
Notwithstanding this increasing device complexity, the basic objective of the analysis remains the same: isolate the detailed physical failure mechanism underlying the electrical failure mode.
A number of first tier isolation techniques such as light emission, voltage contrast, and liquid crystal allow the isolation of the electrical failure mode down to a reasonable number of transistors, in some cases down to a single transistor. However with the technologies quickly shrinking below a 0.5 micron, it becomes important to have second tier isolation techniques with physical isolation resolution down to 500 angstroms or better.
Electron Beam Induced Current (EBIC) is one such technique as it can provide this required fine fault resolution, with the added benefit of being non-destructive with respect to the electrical and physical characteristics of the fault region.

How does it work....magic?

The SEM electron beam generates electron-hole pairs in the semiconductor sample under investigation. Inelastic interaction of the primary electrons with the sample lifts valence electrons into the conduction band, thereby producing free electrons and free holes. A single primary electron can produce 10,000 electron-hole pairs.
In semiconductor devices, the n and p diffusions have a built-in drift field, causing electrons and holes to flow in opposite directions across the junction. This generates an external current that is typically 1000x higher than the beam current. *This substantial charge multiplication effect is the basis for the EBIC technique.*
Sensing of the EBIC current is done using an external current amplifier whose output when mixed with regular secondary electron signal produces an image. This image provides qualitative assessment of subsurface electrical and physical properties within the semiconductor with the resolution of secondary electron imaging.

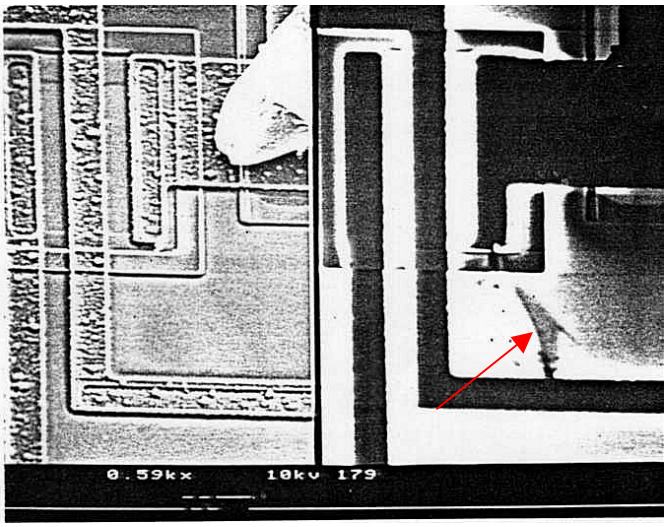

Fig.1 SEM (left) and EBIC (right) photo showing flash-over damage along the surface of the silicon not visible with regular secondary electron imaging.

Junction Defect Detection -

The boundary of the pn junction serves as a transition point for majority carriers where electron beam-induced generation currents originate. As these carriers drift across the junction and recombine, at the current amplifier, the outline of the diffusion becomes delineated. In regions where defects are within the junction (or within a diffusion length of the junction), the recombination will be enhanced and the current production reduced. This results in an attenuation of the EBIC signal into the current amplifier and a dark contrast on the EBIC picture at defect sites.

Further information and videos about EBIC are available at our web site @ http://www.tsi-seminars.com

SEM-EBIC mode of operation is an extremely sensitive technique. It does not require the external application of power to the sample, thereby avoiding secondary damage to the original defect. This contrasts favorably with less sensitive techniques such as Liquid Crystal delineation, which requires significant power dissipation and heat generation, and Voltage Contrast, which requires significant voltage application.

Junction Defect Detection (cont.)-

Fig.2 depicts the sensitivity of the EBIC technique. The EBIC image reveals the location of EOS damage on an input protection diode. A closer look of the image reveals a replica of crystallographic damage, which occurred during thermal runaway. A current filament formed in the high ohmic P- silicon, and current spreading at the transition point of the low ohmic N+ substrate.

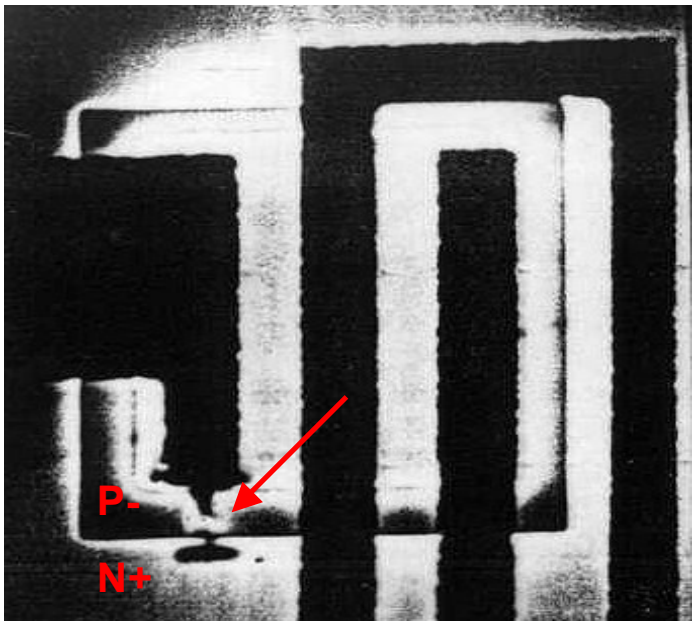

Fig.2 EBIC photo showing EOS damage (arrow); the replicated EBIC images show evidence of thermal runaway.

Oxide Defect Detection-

The evolution of technology has brought about the requirement to analyze and localize defects in very thin gate oxides covered by relatively thick and narrow (submicron) polysilicon traces. Accurate localization of the defect site prior to removal of the polysilicon prevents having to sort out the physical failure mechanism from the etching artifacts introduced during poly removal.

Submicron probing of electrically shorted transistor gates in the SEM is now common place and is used in conjunction with EBIC mode of operation as a powerful second tier isolation tool. Figure 3 shows an example of this technique on a submicron gate.

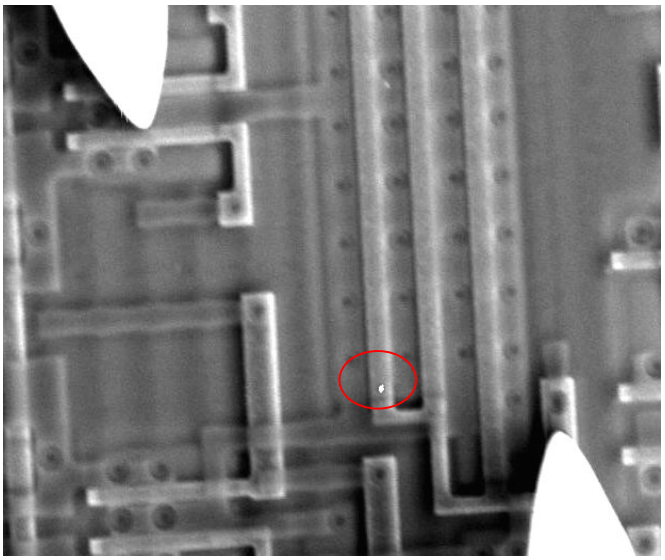

Fig.3 A combination of microprobing in the SEM and EBIC is useful in isolating defects on submicron gates (circle) prior to the removal of the polysilicon.

The detection of oxide defects underneath a polysilicon gate is based upon several factors surrounding the defect site. One prominent factor is whether or not the defect site has a rectifying electrical characteristic for electron-hole pair generation. In the case of pinholes or oxide ruptures, the difference in dopant levels between the polysilicon gate and the underlying silicon often creates a semi-rectifying diode allowing for standard recombination current detection during EBIC analysis.

However, when a non-rectifying electrical characteristic is present, the detection can be accomplished by carefully setting the penetration depth of the electron beam by varying the accelerating voltage. Pinholes or thinning of the gate oxide represent a decrease in thickness. The relative beam penetration depth is higher over these defect areas, which results in higher EBIC current. Controlling the accelerating voltage (=penetration depth), and current gain settings are critical when isolating this type of defect.

Junction Delineation-

The established technique for junction delineation involves the use of chemical stains and etchants. However, in some cases involving lightly doped diffusions, chemical staining results become very interpretive.
EBIC analysis eliminates this interpretation to a large extent allowing straightforward identification of metallurgical junctions as shown in Fig.4.

Subsurface Damage -

EBIC analysis is also very useful in isolating electrical shorts through several layers of metallization where other isolation techniques would fall short, as shown in the case of the HEXFET in Fig.5. In this case, the top source metal plate makes light emission impractical, and liquid crystal difficult due to its heat sinking effects.

Fig. 6 shows an example of isolating an electrical short on a large polysilicon capacitor following the removal of metallization.

Summary -

Like many tools in our failure analysis lab, EBIC analysis is not a catch-all analytical tool that can be used in every instance to isolate a physical failure sites. However, the availability of the SEM to most analysts makes it a versatile, inexpensive tool that can be used to isolate and characterize many different failure mechanisms. Like many tools, its only limits are in the imagination of the analysts.

References:

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3. M.Strizich, B.Wensink, E.Errett "EBIC Observation of Subsurface Damage" ISTFA 1988, pg.225-226
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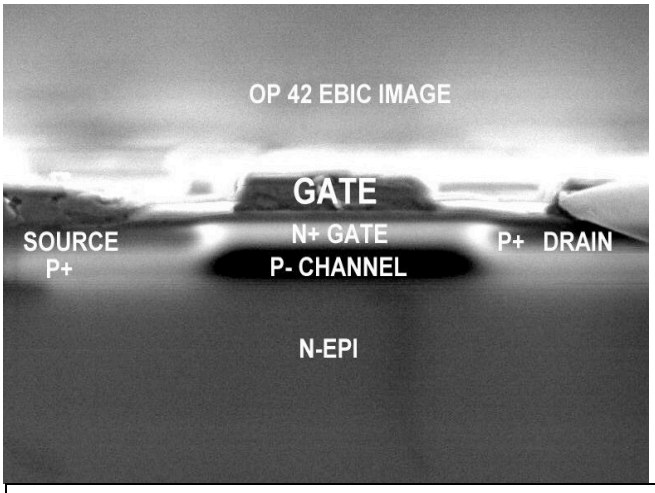

Fig. 4 JFET cross section view showing junction delineation using EBIC.

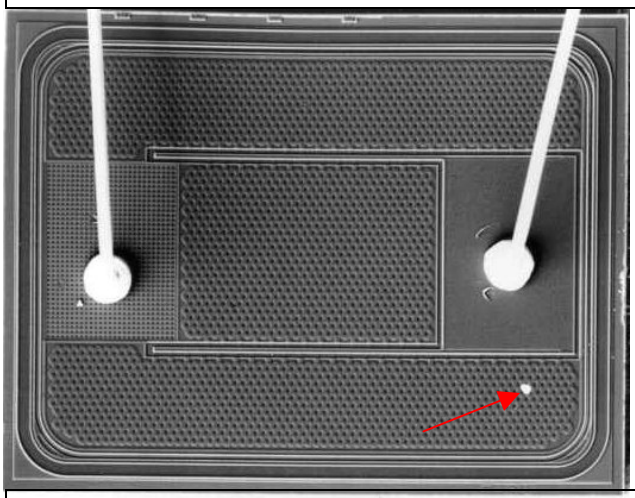

Fig. 5 HEXFET gate short location identified through the top passivation and source metallization plate.

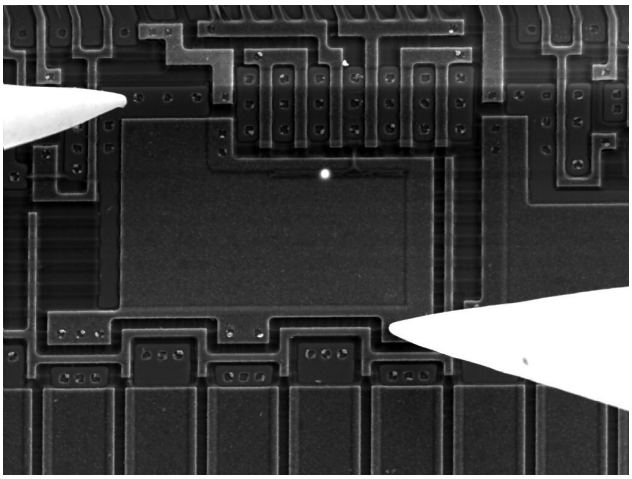

Fig.6 Short location identified on large polysilicon capacitor using EBIC following the removal of the metallization layers.