Voltage Contrast and EBIC Failure Isolation Techniques

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Failure analysis challenges have increased as electronic circuit capability and complexity of integrated circuits evolve to higher densities and smaller feature sizes. Despite this evolution, “old school” tools can be effective in solving problems on both simple and complex devices. In particular, when Voltage Contrast (VC) and Electron Beam Induced Current (EBIC) are combined together results in a powerful analytical technique.

The scanning electron microscope (SEM) is now a standard tool for IC failure analysis with its primary advantage over the light microscope being depth of field and a much higher magnification. This makes isolation techniques that involve the SEM much more favorable than techniques used with the light microscope such as light emission and liquid crystal.

Voltage contrast is typically a first tier failure isolation technique useful in isolating problems to a particular circuit or circuit block. This is particularly valuable when there is a lack of circuit schematics, die maps, logic diagrams or bit maps which can severely limit the amount of useful failure analysis that can be performed. EBIC, on the other hand, is considered a second tier isolation technique which provides information of a more exact failure location, typically down to 500 angstrom resolution. It is particularly powerful when performed using a probe station in the SEM. Not only does EBIC provide this required fine fault resolution, it has the added benefit of being non-destructive with respect to the electrical and physical characteristics of the fault region.

Qualitative Voltage Contrast:

Significant benefits can be obtained using qualitative voltage contrast for not only small and medium scale integrated circuits, but also more complex devices such as large state-of-the-art memory arrays. In addition, it can be used on complex microcontroller based products devices, if the general failure location (circuit block) is known. It is particularly helpful on complex memory devices when no topological bit maps are available. The failing memory address can quickly be found by repeatedly strobing the failing address bit location. This same set-up can be used to extract the topological bit map in the case where reverse engineering of the memory array is required.

Qualitative voltage contrast provides the failure analyst with the ability to observe the logic stages, and operation of integrated circuits. This allows for the location and identification of the failure site to be done more quickly, particularly when the results are compared against known good devices. Image subtraction techniques are often used to help with the failure location identification.

A primary advantage to voltage contrast is its non-destructive and less risky than mechanical probing. For best imaging results the top glassivation is typically removed, however, acceptable results are often obtained with the glassivation on using Charge Coupled Voltage.

The voltage contrast signal is generated by applying an external bias and a clock signal to the device. PC based pattern generators are common place, and easy to interface to just about any SEM.

A resulting voltage potential is applied to the metal lines on the integrated circuit. The contrast is the effect of secondary electrons which are “weak” and easily influenced by the electrical field on the metal stripe. A positive potential on the metal stripe results in a dark

contrast as the number of secondary electron emission is reduced, whereas at 0V a light contrast is observed due to higher secondary electron emission. At lower operating frequencies (khz), a black and white barber stripe can be observed on metal lines which is a direct indication of the logic state, and pattern.

Both SEMs and digital imaging systems have made significant process over the last few years. Systems available today provide the failure analyst much more flexibility for handling one of kind failures. The systems ability to acquire images from both a normal circuit operation using a good device and compare it to the failed device using digital imaging techniques has helped immensely. In addition, PC based pattern generators have made applying stimulus to memory arrays, or more complex integrated circuits straight forward. The new generation of pattern generators are very mobile and easy to interface to an SEM.

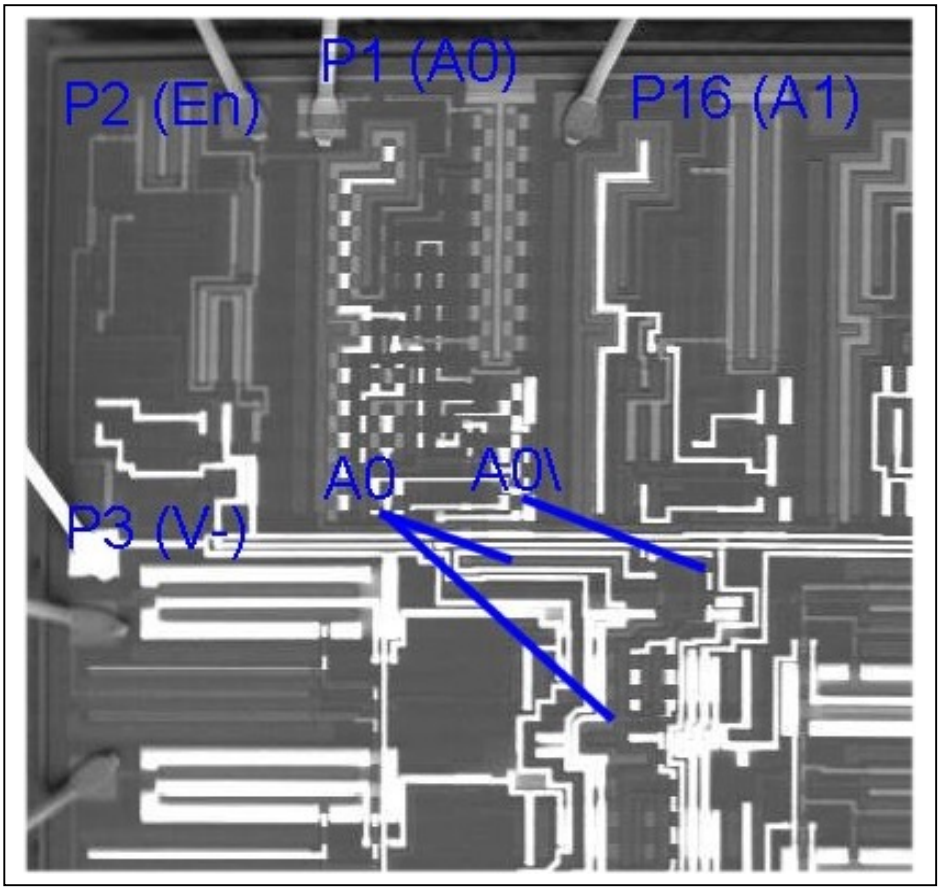

Fig.1
Typical Voltage contrast image showing logic states and voltage patterns that allow circuit operation to be observed.

Electron Beam Induced Current (EBIC):

Following the isolation of the failure site to a particular group of transistors using a first tier isolation technique, a more precise second tier isolation technique like EBIC is required. EBIC has the advantage of good spatial and lateral depth resolution. The lateral depth resolution is controlled by the SEM accelerating voltage.

The SEM electron beam generates electron-hole pairs in the semiconductor sample under investigation. Inelastic interaction of the primary electrons with the sample lifts valence electrons into the conduction band, thereby producing free electrons and free holes. A single primary electron can produce 10,000 electron-hole pairs.

The EBIC current is generated in the semiconductor device near the n and p diffusions which have a built-in drift field, causing electrons and holes to flow in opposite directions across the junction. This generates an external current that is typically 1000x higher than the beam current. This substantial charge multiplication effect is the basis for the EBIC technique.

Sensing of the EBIC current is done using an external current amplifier whose output when mixed with regular secondary electron signal produces an image. This image provides qualitative assessment of subsurface electrical and physical properties within the semiconductor with the resolution of secondary electron imaging.

EBIC analysis is also very useful in isolating electrical shorts through several layers of metallization where other isolation techniques would fall short, such as the case of using light emission or liquid crystal.

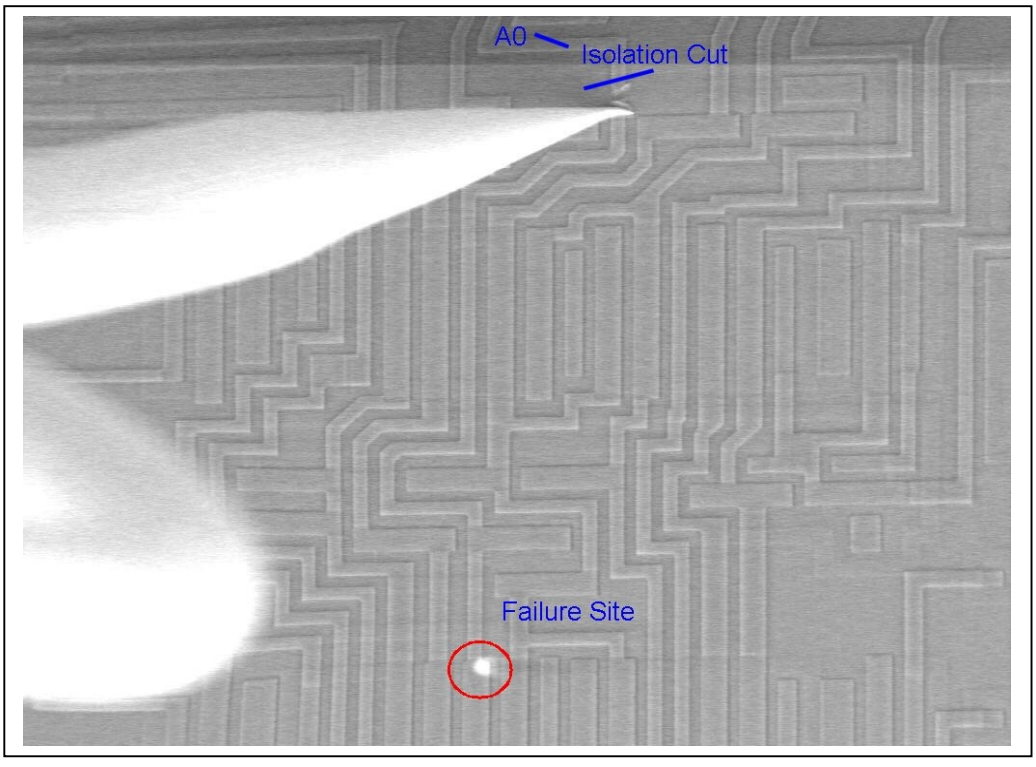

Fig.2
A combination of microprobing in the SEM and EBIC is useful in isolating defects on submicron gates (circle) prior to the removal of the polysilicon.

Memory Array Failure Analysis-

Using a combination of qualitative voltage contrast and EBIC on complex memory arrays is typically a straight forward effective failure analysis approach. Following the localization of the failure site using voltage contrast, albeit a single bit failure, row or column failure, EBIC can be used to isolate the exact failure location. EBIC has the advantage localizing defects in very thin gate oxides covered by relatively thick and narrow (submicron) polysilicon traces.

Accurate localization of the defect site prior to removal of the polysilicon prevents having to sort out the physical failure mechanism from the etching artifacts introduced during poly removal. Submicron probing of electrically shorted transistor gates in the SEM is now common place and is used in conjunction with EBIC mode of operation as a powerful second tier isolation tool during the analysis of complex memory arrays.

The detection of oxide defects underneath a polysilicon gate is based upon several factors surrounding the defect site. One prominent factor is whether or not the defect site has a rectifying electrical characteristic for electron-hole pair generation. In the case of pinholes or oxide ruptures, the difference in dopant levels between the polysilicon gate and the underlying silicon often creates a semi-rectifying diode allowing for standard recombination current detection during EBIC analysis.

However, when a non-rectifying electrical characteristic is present, the detection can be accomplished by carefully setting the penetration depth of the electron beam by varying the accelerating voltage. Pinholes or thinning of the gate oxide represent a decrease in thickness. The relative beam penetration depth is higher over these defect areas, which results in higher EBIC current. Controlling the accelerating voltage (=penetration depth), and current gain settings are critical when isolating this type of defect.

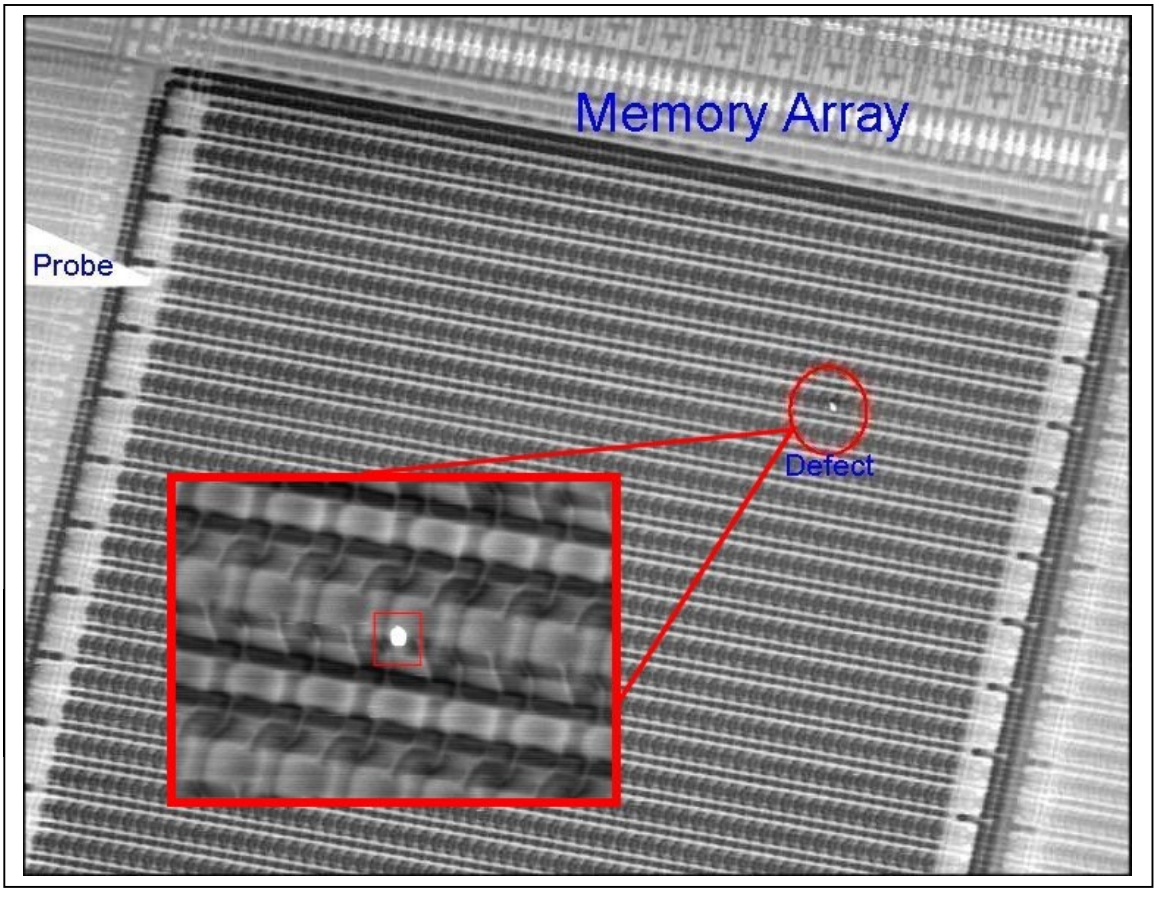

Fig.3
A combination of microprobing in the SEM and EBIC is useful in isolating

Conclusions:

Like many tools in our failure analysis lab, Voltage Contrast and EBIC are not catch-all analytical tool that can be used in every instance to isolate a physical failure sites. However, the availability of the SEM to most analysts makes these versatile, inexpensive tools that can be used to isolate and characterize many different failure mechanisms. Like many tools, its only limits are in the imagination of the analysts.

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