MSI Core Business

License Pix2Net Software Suite

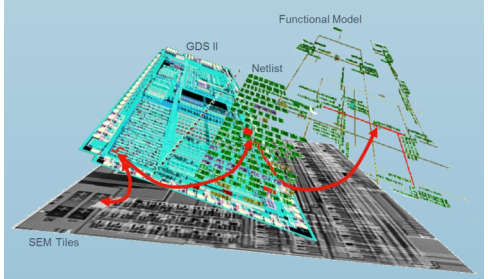
State of the Art IC Reverse Engineering

Electronic Part Obsolescence

Trusted system/Cyber Vulnerability

Anti-Tamper Design & Analysis

IC Patent Infringement



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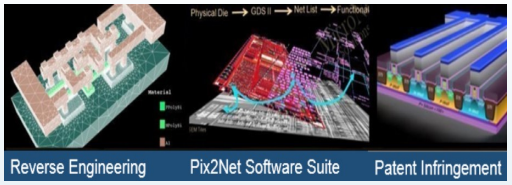
Pix2Net

Software Suite

MSI Newsletter - Oct. 2015

Pix2Net Software Suite……. For Rapid Reverse Engineering of Microelectronics



Pix2Net Software Solutions

Michael Strizich, President MSI Oct. 2015

The Solution.....

MicroNet Solutions Inc. (MSI) *has developed proprietary techniques, and software to reverse engineer complex microcircuits and systems, allowing for complete extraction of functionality and microcode.*

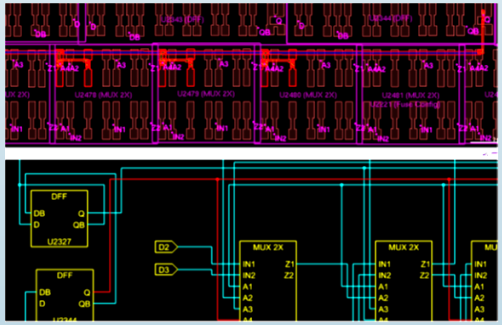
Reverse Engineering state-of-the art microchips is very difficult at best given the small dimensions, density of transistors and number of metal layers (Billions of nodes of information to track).

The Pix2Net software suite features a proprietary software guided stage allowing for accurate SEM tile extraction, and stitching for perfect layer alignment. The GDSII extracted conductive layers are accurately stacked and aligned for circuit connection. Auto Library cell identification, and schematic generation make this the most sophisticated RE software tool on the market.

New Feature –Schematic Capture

The MicroNet Solution.....

The MSI Team *has just released the newest version of Pix2Net Software which allows for real time schematic capture capability. As the library cells are automatically generated and interconnected with the extracted GDS II layers, schematics are composed real-time in a separate window.*



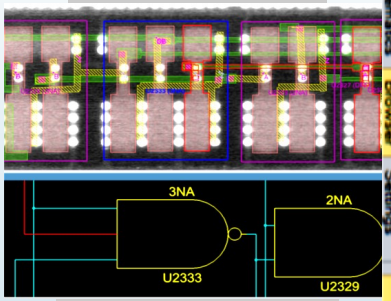
Physical - Schematic Correlation

The schematics have a one on one correlation with the physical net list and library cells . This allows for real time circuit analysis, error checking and circuit modeling.

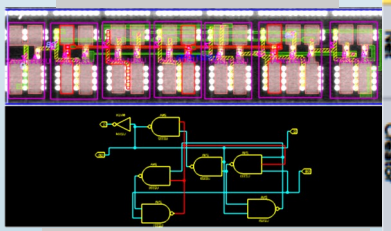
This provides for a considerable time saving while performing reverse engineering for Patent Infringement cases, Electronic Part Obsolescence and vulnerability of Trusted Systems.

Schematic Extraction Flow

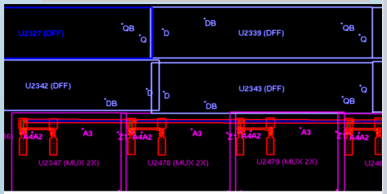
Transistor-Logic Gate



Logic Gate-Library Cell



Library Cell-Logic Circuit



Logic Circuit– Hierarchical Block