# MicroNet
## Solutions Inc.

# *Reverse Engineering  Software and Services*
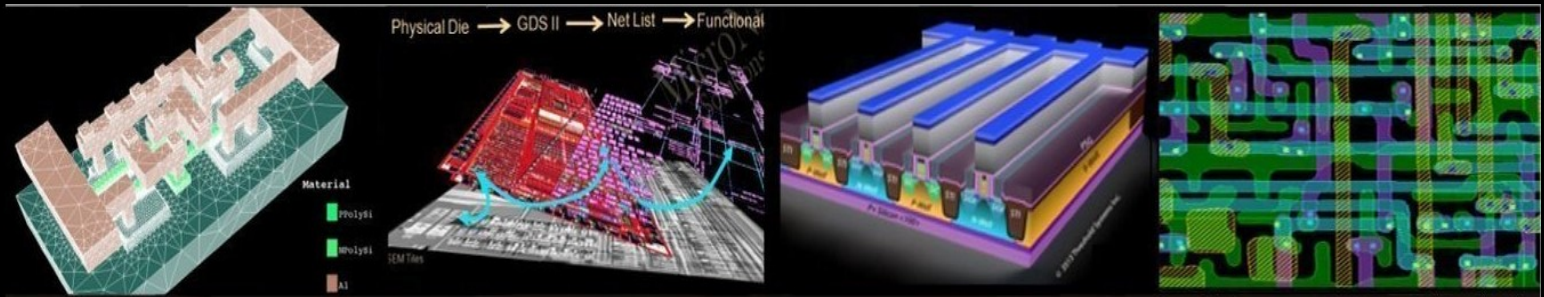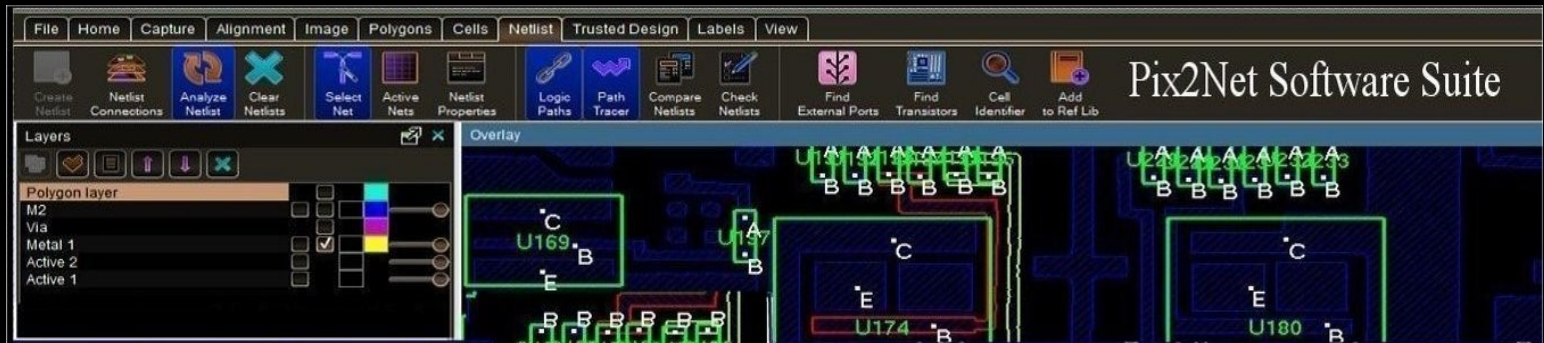




# *Pix2Net Software*

# MicroNet Solutions

## RE Support Ser-

- *Pix2Net Software Suite*
- *Software Customization*
- *Microchip Rev Engineering*
- *PCB Rev Engineering*
- *Technology Rev Engineering*
- *Focus Ion Beam*
  *(Circuit Repair)*
- *Microcode Extraction*
- *Training Services*
- *Backside Laser Probing*
- *Anti-Tamper Design &*
  *Analysis*
- *SEM Mosaics*
- *Sample Preparation*
      *Parallel lapping*
      *Cross sections*

## *The Solution…..*

**MicroNet Solutions Inc. (MSI)** *has over 25 years experience in developing proprietary techniques, and software to reverse engineer complex microcircuits and systems, allowing for complete extraction of functionality and microcode.*

*Reverse Engineering state-of-the art microchips is very difficult at best given the small dimensions, density of transistors and number of metal layers (Billions of nodes of information to track).*

*The Pix2Net software suite features a proprietary software guided stage allowing for accurate SEM tile extraction, and stitching for perfect layer alignment. The GDSII extracted conductive layers are accurately stacked and aligned for circuit connection. Auto Library cell identification, and schematic generation make this the most sophisticated RE software tool on the market.*

www.micronetsol.net

# Pix2Net Software Suite

In the case where select customers would like to perform the work in-house, the Pix2Net software and nano-stage are installed at the customers lab site for a licensing fee. This would include training the customer how to properly delayer the microchips, and use

## Patent Infringement

Services are performed for IC design houses and law firms which specialize in IP representation. Services include complete physical and electrical extraction of circuit layouts, and functionality, to provide evidence for relevant patent claims.

# Electronic Part Obsolescence

Recreate the entire design of a electronic part that has become obsolete, or the design is no longer available. The part can be recreated at the GDS II level, or complete schematic and functional model extraction.

# Pix2Net Software Features

- *Nano Stage - Fits most SEM*
- *Mosaic Stitching*
- *Layer Alignment & Anchor*
- *GDS II Extraction & Editor*
- *Auto Transistor ID*
- *Auto Library Cell Extract*
- *Library Cell Data Base*
- *Cell Pattern Recognition*
- *Net Listing*
- *VHDL, Verilog Spice Models*
- *Auto Schematic Generation*
- *Electrical Error Checking*
- *Polygon Error Checking*
- *Physical to Electrical references*
- *Import & Export GDS II files*
- *Golden GDS II Compare*
- *Memory Auto Extraction*

# Pix2Net Software Suite

**Nano-Stage / Image Capture**

**Polygon (GDS II)**

**Auto Cell Id. / Net List / Schematic**

Multi-Scale Generation
Capture Rotation Alignment
Stitching Manager
Microscope Configuration
Nano-Stage Control
Layer Alignment

Filter (BC. Smooth, Morph)
Clone Polygons
Polygon Editor
Pattern Recognition
Neural Networks
Layer Merge

Library Cell Database
Auto Cell HD & Placement
Netlist (Verilog, VHDL, Spice)
Electrical Short Finder
Logic Error VHDL Checking
Library Cell Instance generation
Auto Cell Instance Placement
Hierarchical Block Manager
Schematic Block Manager
Golden Compare Editor
Generate Transistors
Cell & Port ID.
Find Diffusions

*Stage / Imaging / Stitching*

*GDS II Layer Extraction*

*Circuit Functional Extraction / Schematic*

**Pix2Net Basic**

**Pix2Net Deluxe**

**Pix2Net Premier**

## Basic

Pix2Net Basic comes with a precession Nano-stage stage which interfaces to most SEM's or optical microscopes to obtain very accurate large scale stitched mosaics which can be stacked and aligned. Multi-scale generation makes zoom in  or out viewing very easy.

## Deluxe

Pix2Net Deluxe adds GDS II conversion, polygon editing and cloning features.  Image filtering features allow for the he best obtainable GDS II layer. It also comes with very powerful neural network algorithms for pattern feature recognition.

## Premier

Pix2Net Premier comes complete with circuit extraction features such as auto library cell  identification, auto instance placement and Verilog, VHDL or SPICE net-listing.  Schematics are  automatically built up  as the library cells are laid down.

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